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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,503	10/30/2003	David A. Luick	ROC920020009US1	8053

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IBM Corporation  
Intellectual Property Law  
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EXAMINER
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YU, JAE UN

ART UNIT	PAPER NUMBER
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2185

MAIL DATE	DELIVERY MODE
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04/28/2009

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/697,503	<b>Applicant(s)</b> LUICK, DAVID A.	
	<b>Examiner</b> JAE U. YU	<b>Art Unit</b> 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 14 January 2009.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 2-8, 10-14, 17 and 19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-8, 10-14, 17 and 19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### DETAILED ACTION

The examiner acknowledges the applicant's submission of an amendment dated 1/14/2009.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 2, 3, 6, 10, 11, 14, 17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiarot et al. (US 5,721,864).
2. **Independent claim 19** discloses; “loading a speculative load [**prefetching to L1 cache, Abstract**] into the pipeline [**L1 & L2 cache, Figure 1**]”,  
  
“loading a non-speculative load into the pipeline [**prefetching to L2 cache, Step 240, Figure 2**] a predetermined number of cycles after the action of loading a speculative load [**after determining that the L1 speculative load is a miss, “L1 Miss on Line M”, Figure 2**]”, and  
  
“if the speculative load was a misprediction [**“L1 Miss on Line M”, Figure 2**], then invalidating the speculative load in the pipeline [**not accessing the speculative load in**

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**L1 cache, Figure 2]** and executing the non-speculative load **[executing the L2 load, Step 205 & 206, Figure 2]**, otherwise executing the speculative load and invalidating the non-speculative load **[executing the L1 load, Abstract]**".

3. **Independent claim 17** discloses an invention that is similar in scope as claim 19.

Thus, the claim is rejected by the same reason as claim 19.

4. **Claims 2 and 10** disclose; "the speculative load is loaded in the pipeline **[prefetching to L1 cache, Abstract]**".

5. **Claims 3 and 11** discloses; "one or more of the data loads in the pipeline **[Lines other than the "Line M" in L2, Figure 2]** are not dependent on any specific data load and not selectively flagged".

6. **Claims 6 and 14** disclose; "each flagged instruction is flushed **[cancel instructions, Figure 2]** from the pipeline upon the determination of a misprediction for a data load **["L1 Miss on Line M", Figure 2]**".

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 4, 5, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiarot et al. (US 5,721,864) in view of Au (US 5,548,795).

2. As per **claims 4 and 12**, Chiarot et al. disclose the system and the method recited in claims 17 and 19.

Chiarot et al. do not disclose expressly, “the flag is a bit within the instruction”.

**Au discloses “The D\_Flag fields 308 in each record 202 indicate dependency relative to a more forward command record 202” in column 8, at lines 44-46 and in Figure 3. The dependent commands are executed/inhibited in predetermined order (Abstract).**

Chiarot et al. and Au are analogous art because they are from the same filed of endeavor of processing instructions in a computer system.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Chiarot by executing dependent commands according to the command queue reordering process as taught by Au in the abstract.

The motivation for doing so would have been to process commands in a time and computationally efficient manner as expressly taught by Au in the abstract.

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3. **Claims 5 and 13** disclose, “the flag is attached to the instruction”. Au discloses, in **Figure 3**, the “D\_Flag” field 308 attached to the “Logical Block Address” 302 and 304. The “Logical Block Addresses” correspond to the “data load” from the claim. In addition, examiner notes that mere separation of parts (i.e. flags and data load) is not a patentable distinction over the prior art. See MPEP 2144.04 (C).

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiarot et al. (US 5,721,864) in view of “The Cache Memory Book” by Jim Handy.

5. As per **claim 7**, Chiarot et al. discloses the system recited in claim 17.

Chiarot et al. does not disclose expressly, “a directory”.

In paragraph 27 of the Applicant’s specification, it is disclosed that a directory can be omitted if the cache is a one-way associate or direct-map cache. **Handy discloses a two-way associative cache in Page 54, at lines 23-25.** Since the cache is not a one-way associate or direct-map cache, it inherently includes a directory.

Chiarot et al. and Handy are analogous art because they are from the same field of endeavor of computer storage access/management.

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At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Chiarot et al. by including the two-way associative cache as taught by Handy in Page 54.

The motivation for doing so would have been the high hit rate of the small size two-way associative cache as expressly taught by Handy in Page 55, Figure 2.9.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiarot et al. (US 5,721,864) in view of Sato et al. (US 4,628,450).

7. As per claim 8, Chiarot et al. discloses the system recited in claim 17.

Chiarot et al. does not disclose expressly that the cache "does not include a directory".

Sato et al. discloses **"A set of routines which are frequently used in an OS is stored in a local memory arranged in a CPU and having high-speed elements"** in **column 2, at lines 23-26**, wherein the "local memory" corresponds to the "fast-load data cache" from the claim. Sato et al. also discloses **"A local memory which has part of address locations of the main memory as its address location, which is accessed by a CPU, and which can obtain same effect as cache memory without having cache directory"** in the Abstract.

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Chiarot et al. and Sato et al. are analogous art because they are from the same field of endeavor of computer storage access/management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Chiarot et al. by including the high-speed “local memory” without cache directory as taught by Sato et al. in column 2, at lines 23-26 and in the Abstract.

The motivation for doing so would have been the improved bus performance as expressly taught by Sato et al. in column 2, at lines 27-30.

### ***Arguments Concerning Prior Art Rejections***

#### **1<sup>st</sup> Point of Argument**

Chiarot discloses L1 and L2 cache in Figure 1. Such caches are interpreted as a “pipeline” since a pipeline can be computer components in which an output of a component is provided as an input for another component. Further, Chiarot discloses a pipeline system in column 1, lines 31-40.

#### **2<sup>nd</sup> Point of Argument**

Chiarot loads a non-speculative load after “L1 Miss on Line M” that corresponds to the claimed “predetermined number of cycles”.

#### **3<sup>rd</sup> Point of Argument**



Chiarot discloses flushing instructions in Figure 2. Such instructions are “flagged” since the system has to identify which instructions are to be flushed. Such identification is interpreted as flagging action.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

A. Claims Rejected in the Application

Claims 2-8, 10-14, 17 and 19 have received a second action on the merits and are subject of a second action final.

B. Direction of Future Remarks

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.

If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jae U Yu/

Examiner, Art Unit 2185

4/27/2009

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185